CLAIMS

What is claimed is:

1. An electronic circuit for controlling electron beams from a plurality of field emission cathodes to produce a color image from a television signal onto a phosphor screen of a cathode ray tube (CRT), comprising:

a video memory adapted to receive and store color video information from a video source, the color video information comprising red, green and blue intensity values for each spot to be illuminated on a cathode ray tube (CRT) having a plurality of substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of the red, green and blue phosphor stripes comprise the spots to be illuminated;

the video memory having addressable first, second and third memory portions for storing the red, green and blue intensity values, respectively, wherein the red, green and blue intensity values for a spot are stored at the same corresponding address of the first, second and third memory portions, respectively;

an address counter for selecting memory addresses corresponding to spot locations on the CRT face, the address counter coupled to the video memory;

a color multiplexer having first, second and third inputs coupled to the first, second and third memory portions, respectively, and an output;

a color counter coupled to and controlling the color multiplexer for selecting the red, green and blue intensity values from the video memory, wherein the color counter increments the address counter after each selection sequence of red, green and blue intensity values;

a gate multiplexer have a first input, a second input and an output, the gate multiplexer first input coupled to the color multiplexer output, and the gate multiplexer second input set to a zero intensity value;

a phase counter coupled to and controlling the gate multiplexer, wherein the phase counter switches the gate multiplexer output to the second input having the zero intensity value at each fourth phase count;

an intensity value shift register adapted for receiving intensity values from the gate multiplexer and storing the received intensity values in sequential order, the intensity value shift register comprising a plurality of registers, wherein an input of a first one of the plurality of registers is connected to the output of the gate multiplexer and remaining ones of the plurality of registers each have an output connected to an input of a subsequent one until the subsequent one is a last one of the plurality of registers;

a plurality of digital-to-analog converters (DACs), each of the plurality of DACs having an output adapted for coupling to a respective one of a plurality of field emission cathodes;

a first one of the plurality of DACs having an input coupled to the output of the gate multiplexer, and an input of each of the remaining ones of the plurality of DACs being connected to the output of respective ones of the plurality of registers; and

a video clock having an output coupled to the phase counter and the intensity value shift register, wherein the video clock times when the red, green and blue intensity values for each spot and the zero intensity value between adjacent spots are applied through the plurality of field emission cathodes to the spot portions of the phosphor stripes of the CRT.

2. The apparatus of claim 1, wherein each of the plurality of registers can store an eight bit intensity value.

3. The apparatus of claim 1, further comprising:

first, second and third multipliers for gamma correcting the red, green and blue intensity values, respectively; and

the first, second and third multipliers coupled between the first, second and third memory portions and the first, second and third inputs of the color multiplexer.

4. The apparatus of claim 1, wherein the number of the plurality of DACs is selected from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

5. The apparatus of claim 1, wherein the number of the plurality of registers is selected from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

6. An electronic circuit for controlling electron beams from a plurality of field emission cathodes to produce a color image from a television signal onto a phosphor screen of a cathode ray tube (CRT), comprising:

a color multiplexer adapted for receiving color video information comprising red, green and blue intensity values, the color multiplexer having first, second and third inputs adapted for receiving the red, green and blue intensity values, respectively;

a color counter coupled to and controlling the color multiplexer for selecting the red, green and blue intensity values;

a gate multiplexer have a first input, a second input and an output, the gate multiplexer first input coupled to the color multiplexer output, and the gate multiplexer second input set to a zero intensity value;

a phase counter coupled to and controlling the gate multiplexer, wherein the phase counter switches the gate multiplexer output to the second input having the zero intensity value at each fourth phase count;

an intensity value shift register adapted for receiving intensity values from the gate multiplexer and storing the received intensity values in sequential order, the intensity value shift register comprising a plurality of registers, wherein an input of a first one of the plurality of registers is connected to the output of the gate multiplexer and remaining ones of the plurality of registers each have an output connected to an input of a subsequent one until the subsequent one is a last one of the plurality of registers;

a plurality of digital-to-analog converters (DACs), each of the plurality of DACs having an output adapted for coupling to a respective one of a plurality of field emission cathodes;

a first one of the plurality of DACs having an input coupled to the output of the gate multiplexer, and an input of each of the remaining ones of the plurality of DACs being connected to the output of respective ones of the plurality of registers; and

a video clock having an output coupled to the phase counter and the intensity value shift register, wherein the video clock times when the red, green and blue intensity values for each spot and the zero intensity value between adjacent spots are applied through the plurality of field emission cathodes to the spot portions of the phosphor stripes of the CRT.

7. The apparatus of claim 6, wherein each of the plurality of registers can store an eight bit intensity value.

8. A method for controlling electron beams from a plurality of field emission cathodes to produce a color image from a television signal onto a phosphor screen of a cathode ray tube (CRT), the method comprising the steps of:

providing a video memory adapted to receive and store color video information from a video source, the color video information comprising red, green and blue intensity values for each spot to be illuminated on a cathode ray tube (CRT) having a plurality of substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of the red, green and blue phosphor stripes comprise the spots to be illuminated;

storing the red, green and blue intensity values into first, second and third addressable memory portions, respectively, of the video memory;

selecting memory addresses corresponding to spot locations on the CRT face with an address counter;

providing a color multiplexer having first, second and third inputs coupled to the first, second and third memory portions, respectively, and an output;

selecting the red, green and blue intensity values from the video memory with a color counter coupled to and controlling the color multiplexer, wherein the color counter increments the address counter after each selection sequence of red, green and blue intensity values;

providing a gate multiplexer have a first input, a second input and an output, the gate multiplexer first input coupled to the color multiplexer output, and the gate multiplexer second input set to a zero intensity value;

providing a phase counter coupled to and controlling the gate multiplexer, wherein the phase counter switches the gate multiplexer output to the second input having the zero intensity value at each fourth phase count;

providing an intensity value shift register adapted for receiving intensity values from the gate multiplexer and storing the received intensity values in sequential order, the intensity value shift register comprising a plurality of registers, wherein an input of a first one of the plurality of registers is connected to the output of the gate multiplexer and remaining ones of the plurality of registers each have an output connected to an input of a subsequent one until the subsequent one is a last one of the plurality of registers;

providing a plurality of digital-to-analog converters (DACs), each of the plurality of DACs having an output adapted for coupling to a respective one of a plurality of field emission cathodes;

wherein a first one of the plurality of DACs having an input coupled to the output of the gate multiplexer, and an input of each of the remaining ones of the plurality of DACs being connected to the output of respective ones of the plurality of registers; and

providing a video clock having an output coupled to the phase counter and the intensity value shift register, wherein the video clock times when the red, green and blue intensity values for each spot and the zero intensity value between adjacent spots are applied through the plurality of field emission cathodes to the spot portions of the phosphor stripes of the CRT.

9. A system having an electronic circuit for controlling electron beams from a plurality of field emission cathodes to produce a color image from a television signal onto a phosphor screen of a cathode ray tube (CRT), the system comprising:

a video memory for receiving and storing color video information from a video source, the color video information comprising red, green and blue intensity values for each spot to be illuminated on a cathode ray tube (CRT) having a plurality of substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of the red, green and blue phosphor stripes comprise the spots to be illuminated;

the video memory having addressable first, second and third memory portions for storing the red, green and blue intensity values, respectively, wherein the red, green and blue intensity values for a spot are stored at the same corresponding address of the first, second and third memory portions, respectively;

an address counter for selecting memory addresses corresponding to spot locations on the CRT face, the address counter coupled to the video memory;

a color multiplexer having first, second and third inputs coupled to the first, second and third memory portions, respectively, and an output;

a color counter coupled to and controlling the color multiplexer for selecting the red, green and blue intensity values from the video memory, wherein the color counter increments the address counter after each selection sequence of red, green and blue intensity values;

a gate multiplexer have a first input, a second input and an output, the gate multiplexer first input coupled to the color multiplexer output, and the gate multiplexer second input set to a zero intensity value;

a phase counter coupled to and controlling the gate multiplexer, wherein the phase counter switches the gate multiplexer output to the second input having the zero intensity value at each fourth phase count;

an intensity value shift register adapted for receiving intensity values from the gate multiplexer and storing the received intensity values in sequential order, the intensity value shift register comprising a plurality of registers, wherein an input of a first one of the plurality of registers is connected to the output of the gate multiplexer and remaining ones of the plurality of registers each have an output connected to an input of a subsequent one until the subsequent one is a last one of the plurality of registers;

a plurality of digital-to-analog converters (DACs), each of the plurality of DACs having an output coupled to a respective one of a plurality of field emission cathodes;

a first one of the plurality of DACs having an input coupled to the output of the gate multiplexer, and an input of each of the remaining ones of the plurality of DACs being connected to the output of respective ones of the plurality of registers; and

a video clock having an output coupled to the phase counter and the intensity value shift register, wherein the video clock times when the red, green and blue intensity values for each spot and the zero intensity value between adjacent spots are applied through the plurality of field emission cathodes to the spot portions of the phosphor stripes of the CRT.

10. The system of claim 9, wherein each of the plurality of registers can store an eight bit intensity value.

11. The system of claim 9, further comprising:

first, second and third multipliers for gamma correcting the red, green and blue intensity values, respectively; and

the first, second and third multipliers coupled between the first, second and third memory portions and the first, second and third inputs of the color multiplexer.

12. The system of claim 9, wherein the number of the plurality of DACs is selected from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

13. The system of claim 9, wherein the number of the plurality of registers is selected from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.